**ANSWER THE FOLLOWING**

Got an idea to enhance the structure of Arbiter based PUF to tackle the Machine Learning attacks. We will give the challenge to an **XOR gate** and then implement it in the ordinary Arbiter PUF.

* **What is the I/O Block diagram of your PUF Design?**

Input: challenge (128 or 256 bit) and Diffuse(128 or 256 bit).

Output: Response (128 or 256 bit).

**I/O Diagram** of 1bit diffusion arbiter PUF.

A picture containing screenshot

Description generated with very high confidence

* **How are you going to design for Altera?**

Planning to design the PUF in VHDL and giving a plan to establish the circuit by the Altera FPGA’s Architecture itself. Its internal logic is similar to Arbiter PUF but will contain an additional XOR Gate for better **diffusion.**

This is the code of a 1bit diffusion arbiter PUF:

A screenshot of a cell phone

Description generated with high confidence

* **How will you test it in simulation and on FPGA?**

By writing a VHDL code to get the output in different regions of the Altera FPGA LAB’s must be unique to different regions on the board.

* **How are you going to improve it (to address limitations of another PUF reported in Anderson’s paper)?**

Skipping this question because not using Anderson PUF anymore.

* **What are the real-world applications of your PUF in hardware security implementation?**

**Hardware counterfeiting**: providing license for the hardware device such that the duplicate hardware device doesn’t have the authentication. In this way data won’t be transmitted in an unsecure channel.